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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,235	01/22/2004	Kazuhiro Shimizu	347968US2	2032

22850 7590 12/19/2006

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,235	SHIMIZU, KAZUHIRO	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,9 and 10* is/are rejected.

7)☒ Claim(s) *3-5,7,8 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action (dated 05/03/2006).

Claims 1, 2, 6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terashima (US 5,894,156) in view of Leonardi (US 6,798,037), Kinzer (US 6,608,350) and Ludikhuize (US 5,883,413).

Re claim 1, Terashima discloses a semiconductor device (Fig 12; col 1) comprising:

a semiconductor substrate (1; ln 22) of a first conductivity type (p);

a semiconductor layer (2; ln 22) of a second conductivity type (n) provided on said semiconductor substrate;

a first impurity region (leftmost 3; ln 22) of said first conductivity type (p) provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region (everything right of leftmost 3);

a first isolation structure (rightmost 3) provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region (via substrate 1), extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first

isolation structure and said first impurity region together defining a first isolation region (between 3s) in said RESURF isolation region;

a semiconductor element (rightmost 6) provided in said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region; and

a first MOS transistor (nch RESURF MOSFET; ln 19), comprising

a second impurity region (middle 5) of said second conductivity type (n) provided in said upper surface of said semiconductor layer defined in said first trench isolation region, said second impurity region being connected to a drain electrode (8) of said first MOS transistor,

a third impurity region (leftmost 6) of said first conductivity type (p) provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a first source region (leftmost 5) of said second conductivity type (n) provided in an upper surface of said third impurity region.

Terashima differs from the claimed invention in not disclosing said first isolation structure is a trench isolation structure and in not disclosing a buried impurity region of said second conductivity type provided directly below said second impurity region.

Leonardi discloses (Fig 4) a trench isolation structure (10; col 4 ln 17-20) to be used in any device having junction isolation (col 4 ln 45-59).

Kinzer discloses (Fig 2) a trench isolation structure similar to that of Leonardi, but having outer trench sidewalls doped opposite to the epi layer in which they are formed in order to improve the RESURF effect (col 3 ln 30).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Terashima such that said first impurity region and said first isolation structure each include a trench isolation structure similar to Leonardi, but surrounded by impurity regions similar to Kinzer; at least avoid parasitic effects (Leonardi: col 4 ln 50-53) while improving the RESURF effect.

Ludikhuize discloses (Fig 1) an n-type buried impurity region (18; col 4 ln 33) directly below a second impurity region (6) at the interface between epi layer (4) and substrate (3), higher in concentration (col 4 ln 33) than the epi layer (col 3 ln 45).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Terashima in view of Ludikhuize such that a buried impurity region of said second conductivity type is provided directly below said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer; at least to effectively drain charge corresponding to voltage peaks at the drain (Ludikhuize: col 2 ln 13-19, col 4 ln 33-67).

Re claim 2, Terashima discloses (Fig 12) an isolation structure (rightmost 3) provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region (via 1), extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said isolation structure and said first impurity region together defining an isolation region (between 3s) in said RESURF isolation region.

Terashima differs from the claimed invention in not disclosing a second trench isolation structure.

Leonardi discloses (Fig 4) a trench isolation structure (10; col 4 ln 17-20) comprising plural trench isolation structures (10 made of plural sets 4*5*) not connected to, and separated by a certain distance from, one another.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Terashima in view of Leonardi such that a second trench isolation structure not connected to said first trench isolation structure and separated by a certain distance from said first trench isolation structure is provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure, said first impurity region, and said first trench isolation structure together defining said first trench isolation region in said RESURF isolation region; at least for improved electrical isolation.

Re claim 6, Terashima as modified above discloses (Fig 12) said first trench isolation structure (rightmost 3) reaches said semiconductor substrate (1), and wherein an end portion of said first trench isolation structure reaches a depth shallower than the [greatest possible] depth (same depth as 4) of said buried impurity region.

Re claim 9, Terashima (Fig 12) as modified above discloses all structural limitations of the claimed trench isolation structure and MOS transistor.

Terashima (Fig 12) as modified above differs from the claimed invention in not disclosing a second trench isolation structure and a second MOS transistor.

Terashima (Fig 7) discloses an analogous device having a first and a second isolation structure (separating MOSFETs from island region) provided in a semiconductor layer (12b) defined in a RESURF isolation region and having a first and a second MOS transistor (two nch RESURF MOSFET).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Terashima (Fig 12) as already modified above in view of Terashima (Fig 7) such that it further comprises:

a second trench isolation structure provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region, extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure and said first impurity region together defining a second trench isolation region in said RESURF isolation region, and

a second MOS transistor, comprising

a fourth impurity region of said second conductivity type (n) provided in said upper surface of said semiconductor layer defined in said second trench isolation region, said fourth impurity region being connected to a drain electrode of said first MOS transistor,

a fifth impurity region of said first conductivity type (p) provided in said upper surface of said semiconductor layer defined between said first and fourth impurity regions, and

a second source region of said second conductivity type (n) provided in an upper surface of said fifth impurity region;

at least so a plurality of level shift elements can be connected to one resurf isolation island region (col 8 ln 39-40).

Re claim 10, Terashima discloses (Fig 12; col 1) an interconnect line (8; ln 25) provided over said first trench isolation structure to be electrically connected to said drain electrode (portion of 8 contacting 5 is drain electrode), and

a field plate (11; ln 49) held between said first trench isolation structure and said interconnect line,

wherein said field plate is an electrode which is electrically connected to said semiconductor layer defined in said first trench isolation region (11 is connected to 3 which is connected to 2; col 1 ln 29-31).

Allowable Subject Matter

Claims 3-5, 7, 8, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the references of record, alone or in combination, fail to disclose at least the following limitation required by dependent claims 3, 5, and 7:

"said in-line portion including a plurality of spaced-apart conductive films".

Response to Arguments

Applicant's arguments filed 10/02/2006 with respect to Leonardi have been fully considered but are moot in view of the new ground of rejection.

Applicant's arguments filed 10/02/2006 with respect to Ludikhuize have been fully considered but are not persuasive. As noted by the applicant (reply pg 11), Terashima discloses the claimed depth. Nothing in examiner's modification changes any depth or size; only the interior of the isolation structure and the horizontal location of the buried diffusion region are modified, relative depths remain unchanged.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571- 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
11 July 2006

Douglas W. Owens 12/10/06

DOUGLAS W. OWENS
PRIMARY EXAMINER